

T. Daniel Loveless, Ph.D.
UC Foundation Assistant Professor
 Electrical Engineering Department
 College of Engineering and Computer Science
 University of Tennessee at Chattanooga

I. Contact Information:

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Phone (o):	423-425-2353

II. Education:

Ph.D., Electrical Engineering, Vanderbilt University, August 2009
 GPA: 3.83/4.00, Major GPA: 3.90/4.00

M.S., Electrical Engineering, Vanderbilt University, May 2007
 GPA: 3.79/4.00, Major GPA: 3.88/4.00

B. S., Electrical Engineering, Georgia Institute of Technology, July 2004
 High Honors, GPA: 3.54/4.00, Major GPA: 3.73/4.00

III. Honors, Awards, Service, and Outreach

Honors and Awards

- Best student poster award (2nd place), 52nd Annual Conference of the National Collegiate Honors Council (NCHC), 2017, “Efficacy of Fuzzy Electronics in Space,” S. Singh, T. D. Loveless.
- Named UC Foundation Assistant Professor in recognition of distinguished service as faculty member at UTC, Apr. 2017.
- Recipient of 2016 GigTank365 Summer Fellowship (UTChattSat), *Co.Lab*, Chattanooga, TN, May-July 2016.
- STEM Category Winner in Faculty Elevator Speech Competition, “Rocket Scientist, Engineer, Educator,” *UTC’s Research Dialogues*, Apr. 2016.
- Outstanding Researcher Award, Electrical Engineering, University of Tennessee at Chattanooga, 2015-2016, 2016-2017.
- Received highest ranking of “Exceeds Expectations” three years in a row for service, teaching, and research activities at the University of Tennessee at Chattanooga, 2014-2015, 2015-2016, 2016-2017.
- Elevated to Senior Member, IEEE, June 2015.
- Best student poster award, 37th Annual Government Microcircuit Applications & Critical Technology Conference (GOMACTech), 2012, “Single-Event Hardening Techniques for CMOS Operational Amplifier Design,” Raymond W. Blaine, Nicholas M. Atkinson, Jeffrey S. Kauppila, Sarah E. Armstrong, T. Daniel Loveless, W. Timothy Holman, and Lloyd W. Massengill.
- Best poster award, 2011 International Reliability Physics Symposium (IRPS), “Neutron and Alpha Particle Induced Soft-Error Rates for Flip Flops at a 40 nm Technology Node,” Srikanth Jagannathan, T. D. Loveless, T. Reece, B. L. Bhuvu, S-J. Wen, R. Wong, L. W. Massengill.
- Best paper award, 35th Annual Government Microcircuit Applications & Critical Technology Conference (GOMACTech), 2010, “Recent Advances in Radiation-Hardened-by-Design Analog and Mixed-Signal Circuits,” W.T. Holman, L.W. Massengill, B.L. Bhuvu, A.F. Witulski, and T.D. Loveless.

- Recipient of the 2008 IEEE Nuclear Plasma and Sciences Society (NPSS) Graduate Scholarship Award for contributions to the fields of Nuclear and Plasma Sciences, March 2008.

Outreach

- Project mentor for nine 11th grade students from the Baylor School, “The Use SUAVs for Attacking Malaria,” Oct.-Dec. 2017.
- Project mentor for nine 11th grade students from the STEM High School Fab Lab, “Mitigating Cold-Temperature Effects in High-Altitude Balloon Payloads,” Oct.-Dec. 2016.
- Panelist, The Baylor School Accelerator’s Entrepreneurial Panel, “How to Develop an Idea,” Nov. 2016.
- “The Martian” and “UTChattSat: Engineering for Outer Space in the Classroom,” Outreach Presentations at the Chattanooga Girls Leadership Academy, Chattanooga, TN, Apr. 19, 2016 and Oct. 6, 2016.
- “Minimum Size and Maximum Packing Density of Nonredundant Semiconductor Devices,” Baylor School Journal Club, Feb. 21, 2016.
- Established relationships with Hamilton County Department of Education, the Chattanooga Girls Leadership Academy, and the UTC Challenger STEM Learning Center for development of space science curriculum, Aug. 2015-present.
- Mentor for one East Ridge High School Senior project in electrical engineering, Jan.-May 2015.
- Volunteer for the School for Science and Math at Vanderbilt, a joint venture between Vanderbilt University Medical Center and Metropolitan Nashville Public Schools (MNPS), 2011-2014.
 - Sophomore project mentor, 2012-2013: 1) Microcontroller-driven autonomous bridge inspection bot, 2) Microcontroller-driven autonomous soil moisture measurements through electromagnetic induction, 3) A sense-capacitor-based virus detection circuit, 4) A nano-pipette through electrolysis
 - Engineering panel for Remote Sensing Design Day, 11/20/13

Service

- IT Governance Council, Nov. 2017-present.
- Reviewer, Promoting Equity and Diversity on Campus, Sept. 2017.
- Undergraduate Petitions Committee, Aug. 2017-present.
- CECS Outreach and Research Committee, Jan. 2017-present.
- UTC General Education Steering Committee, Jan. 2017-July 2017.
- High Impact Practices Grant Committee, Aug. 2016-present.
- Search Committees: Director of Student Success, Electrical Engineering Faculty (2), Director of the SimCenter, UTC, Aug. 2016-July 2017.
- Awards committee, 2016 IEEE Nuclear and Space Radiation Effects Conference, May-Sept., 2016.
- Led the Electrical Engineering Department’s efforts in 2015-2016 ABET re-accreditation cycle. Established college-wide methodology for student outcome assessment, Nov. 2015.
- Community liaison for the College of Engineering and Computer Science (CECS) Electrical Engineering Department, Oct. 2015-present
- Chair, College of Engineering and Computer Science (CECS) ABET Taskforce Committee, 2015-2016.
- UTC Departmental Honors Committee, Sept. 2015-Aug. 2016.
- Participant in UTC Roundtable with Bruce Katz, Vice President and Founding Director of the Brookings Institute, Sept. 2015.
- Mentor and Participant on UTC Fellowship Team for 2015 GigTank (boutique accelerator for seed-stage startups developing ultra high-bandwidth business), Chattanooga, TN, June-Aug. 2015.

- Involved in UTC EE Department recruitment efforts at Chattanooga State Community College, Dalton State Community College, and Cleveland State Community College, 2014-present.
- Faculty co-advisor for IEEE, University of Tennessee at Chattanooga, 2014-present
- Session chair: 2014 Nuclear and Space Radiation Effects Conference (Single-Event Effects: Devices and ICs), Paris, FR, July 2014
- Faculty advisor for IEEE Eta Kappa Nu (HKN) Student Honor Society, Epsilon Lambda Chapter (Vanderbilt University), 2013-2014
- Faculty advisor for IEEE Vanderbilt, 2012-2014
 - Started microcontroller design group, Oct. 2013
 - Hosted Arduino “Speed Build” competition, Nov. 2013
- Session chair: 2012 Single Event Effects Symposium, La Jolla, CA, April 2012
- Reviewer for *IEEE TDMR* (2013), *IEEE RADECS* (2013, 2015) *IEEE NSREC* (2013, 2014, 2015, 2017), *HEART Conference* (2011, 2014, 2015, 2016), *Journal of Electronic Testing: Theory and Applications* (2011), *IEEE Sensors* (2010-present), *IEEE NSREC Data Workshop* (2009), *IET Electronics Letters* (2009-present), *IEEE Transactions on Nuclear Science* (2008-present)

Professional Development

- Activity Insight Training, (1.5 professional development hours), Nov. 2017
- MyMediaSite Training, (1 professional development hour), Aug. 2015
- NSF Grants Conference (16 professional development hours), May 2015
- Early adopter of the EAB Student Success Collaborative tool for student advisement, Sept. 2015-present
- ABET Fundamentals of Program Assessment Workshop (7 professional development hours), Baltimore, MD, Nov. 2014.
- Hosted MathWorks MATLAB/Simulink and RaspberryPi Workshop (5 professional development hours), UTC, Chattanooga, TN, Nov. 2014.
- OU Campus Website Training (2 professional development hours), Sept. 2014.

Professional Organizations/Certifications

- Senior Member, IEEE TN Branch: 2000–present
 - IEEE Nuclear Plasma Sciences Society, 2007–present
 - IEEE Circuits and Systems Society, 2007–present
 - IEEE Solid-State Circuits Society, 2015–present
 - IEEE Young Professionals, 2014–present
 - IEEE Smart Grid Community, 2014–present
 - IEEE Software Defined Networks Community, 2014–present
 - IEEE Transportation Electrification Community, 2014–present
- EIT Certification, 2005

Other Honors or Activities

- Recipient of the Georgia Tech Alumni Association Scholarship (2000–2004)
- Study Abroad–Metz, France: Georgia Institute of Technology, May–July 2004
- Faculty Honors (semester 4.0 GPA): Georgia Institute of Technology, 2003
- Eta Kappa Nu ECE Honor Society, Georgia Institute of Technology, 2003
- Dean’s List: Georgia Institute of Technology, Aug. 2000–July 2004

IV. Academic Appointments

UC Foundation Assistant Professor

4/17 – present

Electrical Engineering Department
College of Engineering and Computer Science
University of Tennessee at Chattanooga

Supervisor: Prof. Ahmed Eltom, Professor and Chair, EE Department (Ahmed-Eltom@utc.edu)

- Assistant Professor** 8/14 – 04/17
 Electrical Engineering Department
 College of Engineering and Computer Science
 University of Tennessee at Chattanooga
 Supervisor: Prof. Ahmed Eltom, Professor and Chair, EE Department (Ahmed-Eltom@utc.edu)
- Research Assistant Professor** 10/13 – 7/14
 Department of Electrical Engineering and Computer Science
 Vanderbilt University
 Supervisor: Prof. Dan Fleetwood, Professor and Chair, Department of EECS
 (dan.fleetwood@vanderbilt.edu)
- Adjunct Assistant Professor** 01/11 – 10/13
 Department of Electrical Engineering and Computer Science
 Vanderbilt University
 Supervisor: Prof. Dan Fleetwood, Professor and Chair, Department of EECS
 (dan.fleetwood@vanderbilt.edu)
- Instructor** 06/09 – 07/10
 Department of Electrical Engineering and Computer Science
 Vanderbilt University
 Supervisor: Prof. Dan Fleetwood, Professor and Chair, Department of EECS
 (dan.fleetwood@vanderbilt.edu)
- Invited Lecturer** for: 01/06 – present
 ENEE 4900 (Fundamentals of Engineering and Professionalism), Instructors: Abdul Ofoli,
 Ahmed Eltom, Univ. of Tennessee at Chattanooga
 ENEE 5000 (Graduate Seminar), Instructor: Ahmed Eltom, Univ. of Tennessee at Chattanooga
 EECE 213 (Circuits II), Instructors: Robert A. Reed, Jeff Black, Vanderbilt University
 EECE 285 (VLSI), Instructors: Bharat L. Bhuvu, Art Witulski, Vanderbilt University
 EECE 304 (Radiation Effects and Reliability), Instructor: Dan Fleetwood, Vanderbilt University
 EECE 342 (Advanced Digital Electronics), Instructor: Lloyd Massengill, Vanderbilt University
 EECE 341 (Advanced Analog Electronics), Instructor: Lloyd Massengill, Vanderbilt University
- Graduate Teaching Assistant** 08/05 – 12/05
 Department of Electrical Engineering, Vanderbilt University (EECE 235, Electronics I)
 Instructor: Prof. Weng Poo Kang, Professor, Department of EECS
 (weng.p.kang@Vanderbilt.Edu)

V. Teaching Summary

Advanced Electronics (ENEE 3770), University of Tennessee at Chattanooga

- This course studies advanced concepts in electronics. Topics include the design of practical and ideal operational amplifier circuits for given transfer functions, the design of active filters, the design of non-linear and pulse shaping circuits, and advanced amplifiers.
- Overall ratings (previous 2 semesters). Average rating of 6.77/7.00.
 - 6.60/7.00 (S2015), 6.79/7.00 (S2016), 6.92/7.00 (S2017)
- Average Enrollment: 14
- Student evaluations available upon request

Advanced Electronics Laboratory (ENEE 3770L), University of Tennessee at Chattanooga

- This laboratory consists of a series of projects in advanced electronics culminating in a major design project, all totally designed by the student.
- Overall ratings (previous 2 semesters). Average rating of 6.54/7.00.
 - 6.54/7.00 (*S2015*), 6.54/7.00 (*S2016*)
- Average Enrollment: 7
- Student evaluations available upon request

Group Study (ENEE 4999), University of Tennessee at Chattanooga

- Title: Embedded Systems for Space Applications
- This course is a project-based study of real-time operating systems and embedded applications for space systems. Advanced concepts in microprocessors, sensors, and interfacing will be covered.
- Course recognized as meeting experiential learning criteria and delineated for “Beyond the Classroom” credit at UTC, S2016-present.
- Overall ratings (previous 1 semester). Average rating of 6.34/7.00.
 - 6.34/7.00 (*S2016*), 6.93/7.00 (*S2017*)
- Average Enrollment: 9
- Student evaluations available upon request

Group Study (ENEE 4999), University of Tennessee at Chattanooga

- Title: VLSI Design
- This course is a project-based study of basic theories and techniques of digital and analog VLSI design in CMOS technology. Fundamental concepts and structures of VLSI systems, standard CMOS and bipolar fabrication processes, design rules, interconnect analysis, layout, simulation, and testing are covered.
- Overall ratings (previous 1 semester). Average rating of 6.71/7.00.
 - 6.71/7.00 (*S2015*), N/A (*F2015*)
- Average Enrollment: 2
- Student evaluations available upon request

Group Study (ENEE 5910), University of Tennessee at Chattanooga

- Title: Real-Time Embedded Systems
- This course is a project-based study of real-time operating systems and embedded applications for space systems. Advanced concepts in microprocessors, sensors, and interfacing will be covered.
- Overall ratings (previous 1 semester). Average rating of 6.75/7.00.
 - 6.75/7.00 (*S2015*), (*S2016 in progress*)
- Average Enrollment: 4
- Student evaluations available upon request

Group Study (ENEE 5910), University of Tennessee at Chattanooga

- Title: Advanced Electronics and Integrated Circuits
- This course is a graduate-level course on advanced electronics. Topics include the design of practical and ideal operational amplifier circuits for given transfer functions, the design of active filters, the design of non-linear and pulse shaping circuits. Basic concepts of programmable controllers are discussed. To obtain graduate credit for this course, the student must participate in bi-weekly journal club meetings (to be coordinated with the instructor). The journal club requires each student to suggest a journal article for the group and host a debate. Each student is required to host at least 4 journal club meetings. In each meeting, the host student must provide a brief (no more than 10 minutes) presentation on the important topics of the recommended article, and mediate discussion.
- Overall ratings (previous 1 semester). Average rating of 7.00 /7.00.
 - 7.00/7.00 (S2015)
- Average Enrollment: 1
- Student evaluations available upon request

Group Study (ENEE 5910), University of Tennessee at Chattanooga

- Title: Wireless Embedded Systems
- This course is a graduate-level, project-based course on wireless embedded systems. Students are required to complete a design project and participate in bi-weekly journal club meetings (to be coordinated with the instructor). The journal club requires each student to suggest a journal article for the group and host a debate. Each student is required to host at least 4 journal club meetings. In each meeting, the host student must provide a brief (no more than 10 minutes) presentation on the important topics of the recommended article, and mediate discussion.
- Overall ratings (previous 1 semester). Average rating of 7.00 /7.00.
 - 7.00/7.00 (S2015)
- Average Enrollment: 2
- Student evaluations available upon request

Circuits I (ENEE 2700), University of Tennessee at Chattanooga

- This course discusses the use of basic electrical circuit element models, signal representations, and circuit analysis methods.
- Implemented major course re-design in the fall semester of 2016 to include the following elements: hybrid-flipped classroom (custom lecture videos, online assignments and tracking, in-class one-on-one help sessions, material re-structuring). As a result the mean score of the course increased by approximately 10 point when compared to previous two semesters.
- Overall ratings (previous 3 semesters). Average rating of 6.39/7.00.
 - 6.40/7.00 (F2014), 6.75/7.00 (F2015), 6.01/7.00 (F2016)
- Average Enrollment: 37
- 1 graduate teaching assistant (F2014)
- Student evaluations available upon request

Embedded Systems (ENEE 4710), University of Tennessee at Chattanooga

Microprocessor Applications (ENEE 4700), University of Tennessee at Chattanooga

- This course discusses practical microprocessor principles, programming, interfacing, *and introduction to FPGA (added to description in F2015, hence course number and name change)*. Design of programs for basic data acquisition and control using the microprocessor as a system component.
- Overall ratings (previous 3 semesters). Average rating of 6.51/7.00.
 - 6.46/7.00 (F2014), 6.26/7.00 (F2015), 6.81/7.00 (F2016), F2017 in progress
- Average Enrollment: 27
- Student evaluations available upon request

Introduction to Circuits I (EECE 112), Vanderbilt University

- This course discusses the use of basic electrical circuit element models, signal representations, and circuit analysis methods.
- Overall instructor ratings (6 semesters). Average rating of 4.44.
 - 4.18/5.00 (*Su2009*), 4.27/5.00 (*S2011*), 4.35/5.00 (*F2011*), 4.50/5.00 (*S2012*), 4.64/5.00 (*F2012*), 4.45/5.00 (*S2013*), 4.45/5.00 (*F2013*)
- Overall course ratings (6 semesters). Average rating of 4.01.
 - 4.00/5.00 (*Su2009*), 3.77/5.00 (*S2011*), 4.18/5.00 (*F2011*), 3.74/5.00 (*S2012*), 4.25/5.00 (*F2012*), 4.00/5.00 (*S2013*), 4.09/5.00 (*F2013*)
- Average Enrollment: 69
- 2 graduate teaching assistants, 3 undergraduate graders
- Student evaluations available upon request

Independent Study (EECE 397), Vanderbilt University

- Title: TID response of RF Devices in a 32 nm PDSOI Technology (*Spring 2013, in progress*)
- Enrollment: 1 graduate student
- Description: S-parameters of devices fabricated in a 32 nm PDSOI technology will be measured. Contributions of parasitic elements will be de-embedded from measurements (optimal methods will be evaluated). Select devices will be irradiated.

Independent Study (EECE 397), Vanderbilt University

- Title: Effects of TID on CMOS LNA Architectures (*Summer 2012*)
- Enrollment: 1 graduate student
- Description: Three types of low-noise amplifiers (narrow band common source, and wide-band resistive and common gate) were used to study RF circuit design concepts and to analyze electrical and radiation performance tradeoffs. Specific topics included the definitions and significance of s-parameters and other critical design parameters, impedance matching using passives networks, design optimization methods, causes and effects of non-linearity, and total ionizing dose response.

Independent Study (EECE 204), Vanderbilt University

- Title: Assembly and Measurement of Advanced Integrated Circuits (*Spring 2012*)
- Enrollment: 2 undergraduate students

Independent Study (EECE 397), Vanderbilt University

- Title: The Design of a 6.25 GHz Quadrature Voltage-Controlled Oscillator in a 45 nm SOI Technology (*Fall 2011*)
- Enrollment: 1 graduate student

Thesis Committees (Concluded)

- Nicholas Atkinson, PhD, Aug. 2013, Vanderbilt University
 - Title: System-Level Radiation Hardening of Low-Voltage Analog/Mixed-Signal Circuits
 - Role: Committee member
- Srikanth Jagannathan, PhD, Nov. 2013, Vanderbilt University
 - Title: TID Characterization of High Frequency RF Circuits in Nano-CMOS Technologies
 - Role: Co-advisor, committee member
- Yanran Paula Chen, MS, Jan. 2014, Vanderbilt University
 - Title: Single-Event Characterization of Digitally-Controlled Oscillators (DCOs)
 - Role: Co-advisor, committee member
- Pierre Maillard, PhD, Jan. 2014, Vanderbilt University
 - Title: Single Event Transient Modeling and Mitigation Techniques for Mixed-Signal Delay Locked Loop (DLL) and Clock Circuits
 - Role: Committee member

- MAJ Raymond Blaine, PhD, Mar. 2014, Vanderbilt University
 - Title : The Design of Single-Event Hardened Analog and Mixed-Signal Circuits
 - Role: Committee member
- Rachel C. Quinn, MS, July 2014, Vanderbilt University
 - Title: Characterization of Single Event Upsets in 32 nm SOI Technology using Alpha Particle and Heavy-ion Radiation Sources
 - Role: Co-advisor, committee member
- Trey Reece, PhD, Dec. 2014, Vanderbilt University
 - Title: Assessing and Detecting Malicious Hardware in Integrated Circuits
 - Role: Committee member
- David McPherson, BS, May 2015, Departmental Honors Program, University of Tennessee at Chattanooga
 - Title: BasketBallBot: Education Level Development of a Fuzzy Controller for a Linear Motor under Saturation Limits
 - Role: Committee member
- Nelson Gaspard, PhD, Mar. 2017, Vanderbilt University
 - Title: Single-Event Upset Technology Scaling Trends of Unhardened and Hardened Flip-Flops in Bulk CMOS
 - Role: Committee member
- Ameer Patel, MS, May 2017, University of Tennessee at Chattanooga
 - Title: A Remote-IoT Laboratory for Cyber Physical Systems
 - Role: Advisor

Thesis Committees (Ongoing)

- Saama Davies, *currently pursuing MS*, projected graduation May 2018, University of Tennessee at Chattanooga
 - Title (Tentative): Total-Ionizing Dose in Hybrid-Si Photonic Integrated Circuits
 - Role: Advisor
- Matthew Joplin, *currently pursuing MS*, projected graduation May 2018, University of Tennessee at Chattanooga
 - Title (Tentative): Mapping Total-Ionizing Dose Degradation Curves in Microcontroller Peripherals
 - Role: Advisor
- Xiaowen Wang, *currently pursuing PhD*, projected graduation 2018, Vanderbilt University
 - Title: Fault-tolerant timing speculation based on circuit dynamic behavior for improved performance and efficiency in digital system
 - Role: Committee member
- Rachel C. Quinn, *currently pursuing PhD*, projected graduation 2018, Vanderbilt University
 - Title (Tentative): Radiation Hardening of Sequential Logic in FinFET Technologies
 - Role: Committee member
- Yanran Paula Chen, *currently pursuing PhD*, projected graduation 2018, Vanderbilt University
 - Title (Tentative): Single-Event Hardening of Digital Phase-Locked Loops
 - Role: Committee member

Other Advisement

- Jeffrey A. Maharrey, MS, May 2014, Vanderbilt University
 - Title: Characterization of Heavy-Ion Induced Single Event Transients in 32nm and 45nm Silicon-on-Insulator Technologies
 - Role: Co-advisor, mentor

- Ellis Richards, Undergraduate Research Assistant, S2016, University of Tennessee at Chattanooga
 - Title: Radiation Effects in Photonic Integrated Circuits
 - Role: Advisor
- Josh Chapman, Undergraduate Research Assistant, S2016, University of Tennessee at Chattanooga
 - Title: Autonomous Rail Transport Vehicle
 - Role: Advisor

VI. Relevant Work Experience:

Staff Engineer II (Senior Research Engineer) 09/09 – 10/13

Institute for Space and Defense Electronics, Vanderbilt University

Supervisors: **Prof. Lloyd Massengill (lloyd.massengill@vanderbilt.edu)**

Prof. Ron Shrimpf (ron.schrimpf@vanderbilt.edu)

- Provide engineering support including the design, analysis, and test of state-of-the-art technologies for commercial, aerospace, and military customers. Customers include, but not limited to Cisco Systems, BAE Systems, Navy, and Air Force.
- Lead and assist in sponsored research activities, including grant applications. Primary financial support through DTRA and NASA EPSCoR.
- Involved in multi-project, multi-task programming and/or engineering in support of department's projects.
- PI, Co-PI, or Technical Lead on projects totaling over \$4 million in funding.
- Increased ISDE's integrated circuit design and fabrication capability by approximately 400%. Near 100% first-pass success rate in design of sub-100nm CMOS technologies. Instrumental in the design of the Vanderbilt/ISDE test coupon, a standard approach for analysis of radiation effects in advanced CMOS technologies. Technologies include, but are not limited to:
 - TSMC 40 nm, 28 nm, and 20 nm Bulk CMOS
 - IBM 180 nm, 130 nm, 90 nm, and 65 nm Bulk CMOS
 - IBM 45 nm, 32 nm SOI CMOS
 - IBM 14 nm SOI FinFET

Graduate Research Assistant 01/06 – 08/09

Radiation Effects and Reliability Group

Department of Electrical Engineering and Computer Science

Vanderbilt University

Advisor: **Prof. Lloyd Massengill (lloyd.massengill@vanderbilt.edu)**

- Ph.D. Dissertation: "A Generalized Single-Event Analysis and Hardening Options for Mixed-Signal Phase-Locked Loop Circuits," Vanderbilt University, Aug. 2009
- M.S. Thesis: "A Single-Event-Hardened Charge Pump for Phase-Locked-Loop Circuits," Vanderbilt University, May 2007
- Investigation and characterization of single-event effects in phase-locked loop circuits (experimental and theoretical)
- Responsible for the development of:
 - Novel design parameters for single transient mitigation in phase-locked loops
 - Analytical models for error propagation and design of phase-locked loop circuits
 - Radiation-hardened-by-design solutions and guidelines for mixed-signal integrated circuits
- Chip tape-outs:
 - Radiation hardened-by-design 200 MHz charge pump PLLs, IBM 130 nm 8RF process through MOSIS (Dec. 2005)
 - Radiation hardened-by-design 400 MHz and 1.2 GHz charge pump PLLs, IBM 90 nm 9SF process through MOSIS (May 2006)
 - Cyclic redundancy checker, AMI 0.5 μm process through MOSIS (Dec. 07)

- Integer-N frequency dividers using CMOS and current-mode logic, MIT-Lincoln Labs 150 nm 3-dimensional SOI (Nov. 2008)
- Radiation-hardened-by-design programmable clock generator and IC driver circuit (max speed 6 GHz), TSMC 45 nm bulk CMOS (Oct. 2009)
- Radiation effects testing experience:
 - Naval Research Laboratory: Two-photon absorption laser absorption for single-event transient characterization and 2-dimensional single-event upset/transient mapping of 130 nm phase-locked loop and voltage-controlled oscillator circuits, Jan. 2007, May 2007, June 2008, April 2009
 - Naval Research Laboratory: Two-photon absorption laser absorption for hardware Trojan detection and substrate well mapping, April 2009.
 - Lawrence Berkeley National Laboratory: Heavy-Ion induced single-event upset characterization of phase-locked loop circuits, June 2008
- Research proposal accepted for the Semiconductor Research Corporation's (SRC) IC Design Competition, 2007 (Phase One/Two Participant): *A Soft Error Hardened Pipelined Analog-to-Digital Converter and Phase-Locked Loop*

Intern 2001 – 2003

Transmission Power Supply/Electric Systems Operations/Control Support Systems
Tennessee Valley Authority

Supervisor: **Russell Robertson**

- Developed various applications/programs in support of the electric transmission network model

VII. Consulting

Edwin Bohr, Electronics, Inc. 2017

Supervisor: **Bryan Grillone (bgrillone@bohr.com)**

- Embedded systems design consultant

Nu-Trek, Inc. 2017

Supervisor: **Miriam Rauch (lloyd.massengill@reliablemicrosystems.com)**

- Radiation effects test and design consultant

Reliable Microsystems 2016-present

Supervisor: **Lloyd Massengill (lloyd.massengill@reliablemicrosystems.com)**

- RF and high-speed digital design consultant

ParkParrot 2014

Supervisor: **Chandler Burke (wchandlerburke@gmail.com)**

- Led design and prototyping of wireless ultrasonic transceiver

Suntronics, Inc. 2011

Supervisor: **Sam Rainwater (SLH2OH2O@aol.com)**

- Provided engineering support on the radiation testing of PLL sub-circuits, and analysis of acquired data for the evaluation of use in a Satellite Communications System.
- Required travel to Mesa, AZ for business meetings and Texas A&M University for radiation testing

VIII. Research Support/Grants

- (1) **Air Force Phase II SBIR, Sub-Contract to Nu-Trek, Inc. (8/17 – 11/18)**
 Title: Characterization of Radiation Effects in a 180 nm Low-Resistance Semiconductor Process at Cryogenic Temperatures
 Budget: \$110,000
 Role: Principal Investigator
 Percent Responsibility: 37.5% CY
 Graduate Students: 1
- (2) **Center for Excellence in Applied Computational Science & Engineering (CEACSE), Tennessee Higher Education Commission (8/17 – 7/18)**
 Title: Unlocking the Secrets of RF-DNA Fingerprinting
 Budget: \$92,000
 Role: Co-Principal Investigator
 Percent Responsibility: 12.5% CY
 Graduate Students: 2
- (3) **Defense Threat Reduction Agency (DTRA) Sub-contract to Vanderbilt University (10/16 – 10/17)**
 Title: Fundamental Research into Radiation Resiliency of Emerging Circuit Technologies Appropriate to the CWMD Mission
 Budget: \$74,964
 Role: Principal Investigator
 Percent Responsibility: 16.7% CY
 Graduate Students: 1
- (4) **Center for Excellence in Applied Computational Science & Engineering (CEACSE), Tennessee Higher Education Commission (8/16 – 7/17)**
 Title: Modeling Space and Defense Environmental Effects in Emerging Integrated Circuit Technologies
 Budget: \$25,000
 Role: Principal Investigator
 Percent Responsibility: 8.3% CY
 Graduate Students: 1
- (5) **Center for Excellence in Applied Computational Science & Engineering (CEACSE), Tennessee Higher Education Commission (8/16 – 7/17)**
 Title: Smart Buildings through Smarter Models
 Budget: \$99,753
 Role: Principal Investigator
 Percent Responsibility: 12.5% CY
 Graduate Students: 2
- (6) **Provost Student Research Award, The University of Tennessee at Chattanooga (7/15 – 6/16)**
 Title: Radiation Hardening of Low-Voltage Analog and Mixed-Signal Circuits in Sub-32 nm Technology Nodes
 Budget: \$1,000
 Role: Faculty Advisor
 Percent Responsibility: 0% CY
 Undergraduate Student: 1 (Mathew Joplin)

- (7) Defense Threat Reduction Agency (DTRA)**
Sub-contract to Vanderbilt University (1/15 – 7/16)
 Title: Radiation Hardening of Low-Voltage Analog and Mixed-Signal Circuits in Sub-32 nm Technology Nodes
 Budget: \$72,888
 Role: Principal Investigator
 Percent Responsibility: 27.25% CY
 Graduate Students: 1
- (8) Defense Threat Reduction Agency (DTRA) (08/13 – 7/16)**
 Title: Characterization and Mitigation of Nanoscale CMOS
 Budget: \$2,500,175
 Role: Project Manager
 Percent Responsibility: 21.75% CY
 Graduate Students: 3
- (9) BAE Systems (11/13-9/14)**
 Title: Testing and Analysis of a High Performance Quadrature Phase-Locked Loop
 Budget: \$354,266
 Role: Principal Investigator
 Percent Responsibility: 15% CY
 Graduate Students: 0
- (10) BAE Systems (8/11-3/13)**
 Title: Radiation Effects Simulation/Modeling for Ultra Deep Submicron Microelectronics
 Budget: \$440,261
 Role: Technical Lead
 Percent Responsibility: 15% CY
Note: Responsible for \$196,267.00 five month contract extension
 Graduate Students: 0
- (11) Honeywell, Inc. (7/12-5/13)**
 Title: Radiation Effects Analysis of HX5000 Technology
 Budget: \$174,450
 Role: Engineering Support
 Percent Responsibility: 23% CY
 Graduate Students: 0
- (12) Aero Thermo / Navy (1/13-12/15)**
 Title: SSP D5LE Program Support
 Budget: \$2,248,245
 Role: Engineering Support
 Percent Responsibility: 5% CY
 Graduate Students: 0.5
- (13) National Aeronautics and Space Administration (NASA) (2011-2013)**
 Title: Experimental Program to Stimulate Competitive Research (EPSCoR): RadFxSat- A University Based Satellite Program to Study Radiation Effects on Advanced Nanoelectronics
 Budget: \$749,952.00
 Role: Co-Investigator
 Percent Responsibility: 5% CY
 Graduate Students: 1
 Undergraduate Students: 4

(14) Ridgetop Group, Inc., U.S. Air Force (2010)

Title: Test Structure Layout for IBM 45nm TAPO SOI IC Fabrication Run

Budget: \$26,576, 10 months

Role: Principal Investigator

Percent Responsibility: 15% CY

Graduate Students: 0

(15) Boeing Aerospace, Inc. (8/12-12/13)

Title: Boeing/DTRA Rad Hard by Design (RHBD) Phase 3 Task: Single Event Simulations in 45 nm SOI CMOS Technology

Budget: \$671,190

Role: Engineering Support

Percent Responsibility: 15.36% CY

Graduate Students: 4

(16) Cisco Systems, 10 Party Sponsorship (8/12-3/15)

Title: TSMC 20 nm Logic Test Chip Design and Test

Budget: \$893,616

Role: Engineering Support

Percent Responsibility: 12.82% CY

Graduate Students: 4

(17) Robust Chip / DTRA (8/12-8/14)

Title: Solutions for Single-Event Error in Ultra Deep Submicron Semiconductor Technologies Using Simulation

Budget: \$259,885

Role: Technical Lead

Percent Responsibility: 11.22% CY

Graduate Students: 4

(18) Defense Threat Reduction Agency (DTRA) (4/09-9/13)

Title: Characterization and Mitigation of Single Event Effects

Budget: \$2,850,000

Role: Technical Lead

Percent Responsibility: 5% CY

Graduate Students: 4

(19) Cisco Systems, 6 Party Sponsorship (8/10-8/13)

Title: Soft Error Analysis of Designs at 28 nm Platform

Budget: \$525,000

Role: Engineering Support

Percent Responsibility: 2% CY

Graduate Students: 3

IX. Selected Skills:

- Embedded systems based on field-programmable gate arrays (FPGAs), microprocessors and microcontrollers, and systems-on-chip
- CubeSat design
- Digital, analog, and mixed-signal design
- RF communications theory and design
- Integrated circuit design & layout: Cadence Virtuoso, L-Edit
- Use of advanced computing clusters for parallel simulation of devices and circuits
- Printed circuit board design and RF design/testing
- Circuit CAD applications: Cadence, SPICE, Spectre, SpectreRF
- Programming: Matlab, Mathematica, Python, Bash, VHDL, Verilog, Assembly, and others
- Other: Proficient in UNIX, electronic circuit-analysis instrumentation, data collection and analysis/correlation, analog and digital circuit modeling and simulation, design documentation and technical writing

X. Selected Courses:

Digital Integrated Circuit Design, Analog Integrated Circuit Design, RF Circuit Design, Microelectronic Circuits, Semiconductor Devices, Radiation Effects and Reliability, VLSI, Microprocessor Applications, Embedded Systems, Advanced Electronics

XI. Publications:

Total number of publications: 85 (68 refereed articles/proceedings, 12 non-refereed proceedings, 2 theses, 3 book chapters)

Google Scholar **h-index of 19**; **i10-index of 33**; ≥ 1158 total citations; average of >13 citations per article; 101 citations for (J32), 86 citations for (J46), 80 citations for (J30), 73 citations for (J44), 58 citations for (J45), 56 citations for (J20)

Citations per year:

Year	Number of Citations
2007	4
2008	7
2009	52
2010	45
2011	61
2012	74
2013	124
2014	168
2015	261
2016	205
2017	133

Key: **BOLD** indicates my name, Underline indicates student author

Refereed Journal Articles (46)

- (J1) Y. P. Chen, L. W. Massengill, A. L. Sternberg, E. X. Zhang, J. S. Kauppila, M. Yao, A. L. Amort, B. L. Bhuvu, W. T. Holman, and **T. D. Loveless**, "Time-Domain Modeling of All-Digital PLLs (ADPLLs) to Single-Event Upset (SEU) Perturbations," *IEEE Trans. Nucl. Sci.*, vol. PP, no. 99, pp. 1-1, Nov. 2017.
- (J2) R. C. Harrington, J. S. Kauppila, K. M. Warren, Y. P. Chen, J. A. Maharrey, T. D. Haeffner, **T. D. Loveless**, B. L. Bhuvu, M. Bounasser, K. Lilja, and L. W. Massengill, "Estimating Single-Event Logic Cross Sections in Advanced Technologies," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 8, pp. 2115-2121, Aug. 2017.
- (J3) Y. P. Chen, L. W. Massengill, J. S. Kauppila, B. L. Bhuvu, W. T. Holman, and **T. D. Loveless**, "Single-Event Characterization of Common 1st and 2nd-Order All-Digital Phase-Locked Loops (ADPLLs)," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 8, pp. 2144-2151, Aug. 2017.
- (J4) **T. D. Loveless**, S. Jagannathan, E. X. Zhang, D. Fleetwood, J. Kauppila, L. W. Massengill, "Combined Effects of Total Ionizing Dose and Temperature on a K-band Quadrature LC-Tank VCO in a 32 nm CMOS SOI Technology," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 204-211, Jan. 2017.
- (J5) Y. P. Chen, **T. D. Loveless**, A. L. Sternberg, E. X. Zhang, J. S. Kauppila, B. L. Bhuvu, W. T. Holman, M. L. Alles, R. A. Reed, R. D. Schrimpf, D. McMorrow, and L. W. Massengill, "Persistent Laser-Induced Leakage in a 20 nm Charge-Pump Phase-Locked Loop (PLL)," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 512-518, Jan. 2017.
- (J6) Y. P. Chen, L. W. Massengill, B. L. Bhuvu, W. T. Holman, **T. D. Loveless**, W. H. Robinson, N. J. Gaspard, and A. F. Witulski, "Single-Event Characterization of Bang-Bang All-Digital Phase-Locked Loops (ADPLLs)," vol. 62, no. 6, pp. 2650-2656, Dec. 2015.

- (J7) K. J. Shetler, N. M. Atkinson, W. T. Holman, J. S. Kauppila, **T. D. Loveless**, A. F. Witulski, B. L. Bhuvu, E. X. Zhang, and L. W. Massengill, "Radiation Hardening of Voltage References Using Chopper Stabilization," vol. 62, no. 6, pp. 3064-3071, Dec. 2015.
- (J8) J. S. Kauppila, L. W. Massengill, D. R. Ball, M. L. Alles, R. D. Schrimpf, **T. D. Loveless**, J. Maharrey, R. C. Quinn, J. D. Rowe, "Geometry-Aware Single-Event Enabled Compact Models for Sub-50 nm Partially Depleted Silicon-on-Insulator Technologies," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 4, pp. 1589-1598, Aug. 2015.
- (J9) T. D. Haeffner, **T. D. Loveless**, E. X. Zhang, A. L. Sternberg, S. Jagannathan, R. D. Schrimpf, J. S. Kauppila, M. L. Alles, D. M. Fleetwood, L. W. Massengill, and N. F. Haddad, "Irradiation and Temperature Effects for a 32 nm RF Silicon-on-Insulator CMOS Process," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3037-3042, Dec. 2014.
- (J10) Y. P. Chen, **T. D. Loveless**, P. Maillard, N. J. Gaspard, S. Jagannathan, A. L. Sternberg, E. X. Zhang, A. F. Witulski, B. L. Bhuvu, W. T. Holman, and L. W. Massengill, "Single-Event Transient Induced Harmonic Errors in Digitally Controlled Ring Oscillators," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3163-3170, Dec. 2014.
- (J11) N. N. Mahatme, N. J. Gaspard, T. Assis, I. Chatterjee, **T. D. Loveless**, B. L. Bhuvu, W. H. Robinson, L. W. Massengill, S.-J. Wen, R. Wong, "Kernel-Based Circuit Partition Approach to Mitigate Combinational Logic Soft Errors," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3274-3281, Dec. 2014.
- (J12) N. M. Atkinson, W. T. Holman, J. S. Kauppila, **T. D. Loveless**, N. C. Hooten, A. F. Witulski, B. L. Bhuvu, L. W. Massengill, E. X. Zhang, and J. H. Warner, "The Quad-Path Hardening Technique for Switched-Capacitor Circuits," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4356-4361, Dec. 2013.
- (J13) Z. J. Diggins, N. J. Gaspard, N. N. Mahatme, S. Jagannathan, **T. D. Loveless**, T. R. Reece, B. L. Bhuvu, A. F. Witulski, L. W. Massengill, S.-J. Wen, and R. Wong, "Scalability of Capacitive Hardening for Flip-Flops in Advanced Technology Nodes," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4394-4398, Dec. 2013.
- (J14) N. J. Gaspard, S. Jagannathan, Z. J. Diggins, M. P. King, S.-J. Wen, R. Wong, **T. D. Loveless**, K. Lilja, M. Bounasser, T. Reece, A. F. Witulski, W. T. Holman, B. L. Bhuvu, and L. W. Massengill, "Technology Scaling Comparison of Flip-Flop Heavy-Ion Single-Event Upset Cross Sections," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4368-4373, Dec. 2013.
- (J15) S. Jagannathan, **T. D. Loveless**, E. X. Zhang, D. M. Fleetwood, R. D. Schrimpf, T. D. Haeffner, J. S. Kauppila, N. Mahatme, B. L. Bhuvu, M. L. Alles, W. T. Holman, A. F. Witulski, and L. W. Massengill, "Sensitivity of High-Frequency RF Circuits to Total Ionizing Dose Degradation," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4498-4504, Dec. 2013.
- (J16) J. A. Maharrey, R. C. Quinn, **T. D. Loveless**, J. S. Kauppila, S. Jagannathan, N. M. Atkinson, N. J. Gaspard, E. X. Zhang, M. L. Alles, B. L. Bhuvu, W. T. Holman, and L. W. Massengill, "Effect of Device Variants in 32 nm and 45 nm SOI on SET Pulse Distributions," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4399-4404, Dec. 2013.
- (J17) N. N. Mahatme, N. J. Gaspard, S. Jagannathan, **T. D. Loveless**, B. L. Bhuvu, W. H. Robinson, L. W. Massengill, S.-J. Wen, and R. Wong, "Impact of Supply Voltage and Frequency on the Soft Error Rate of Logic Circuits," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4200-4206, Dec. 2013.

- (J18) P. Maillard, W. T. Holman, **T. D. Loveless**, and L. W. Massengill, "A New Error Correction Circuit for Delay Locked Loops," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4387-4393, Dec. 2013.
- (J19) N. N. Mahatme, N. J. Gaspard, S. Jagannathan, **T. D. Loveless**, I. Chatterjee, B. L. Bhuvu, L. W. Massengill, and R. D. Schrimpf, "Experimental Estimation of the Window of Vulnerability for Logic Circuits," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 4, pp. 2691-2696, Aug. 2013.
- (J20) K. Lilja, M. Bounasser, S.-J. Wen, R. Wong, J. Holst, N. Gaspard, S. Jagannathan, **D. Loveless**, and B. Bhuvu, "Single-Event Performance and Layout Optimization of Flip-Flops in a 28-nm Bulk Technology," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 4, pp. 2782-2788, Aug. 2013.
- (J21) N. M. Atkinson, R. W. Blaine, J. S. Kauppila, S. E. Armstrong, **T. D. Loveless**, N. C. Hooten, W. T. Holman, L. W. Massengill, and J. H. Warner, "RHBD Technique for Single-Event Charge Cancellation in Folded-Cascode Amplifiers," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 4, pp. 2756-2761, Aug. 2013.
- (J22) A. V. Kauppila, B. L. Bhuvu, **T. D. Loveless**, S. Jagannathan, N. J. Gaspard, J. S. Kauppila, L. W. Massengill, S.-J. Wen, R. Wong, G. L. Vaughn, and W. T. Holman, "Effect of Negative Bias Temperature Instability on the Single Event Upset Response of 40 nm Flip-Flops," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2651-2657, Dec. 2012.
- (J23) **T. D. Loveless**, J. S. Kauppila, S. Jagannathan, D. R. Ball, J. D. Rowe, N. J. Gaspard, N. M. Atkinson, R. W. Blaine, T. R. Reece, J. R. Ahlbin, T. D. Haeffner, M. L. Alles, W. T. Holman, B. L. Bhuvu, L. W. Massengill, "On-Chip Measurement of Single-Event Transients in a 45 nm Silicon-on-Insulator Technology," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2748-2755, Dec. 2012.
- (J24) S. Jagannathan, **T. D. Loveless**, B. L. Bhuvu, N. J. Gaspard, N. Mahatme, T. Assis, S.-J. Wen, R. Wong, and L. W. Massengill, "Frequency Dependence of Alpha-Particle Induced Soft Error Rates of Flip-Flops in 40-nm CMOS Technology," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2796-2802, Dec. 2012.
- (J25) R. W. Blaine, N. M. Atkinson, J. S. Kauppila, S. E. Armstrong, N. C. Hooten, **T. D. Loveless**, J. H. Warner, W. T. Holman, L. W. Massengill, "Differential Charge Cancellation (DCC) Layout as an RHBD Technique for Bulk CMOS Differential Circuit Design," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2867-2871, Dec. 2012.
- (J26) R. W. Blaine, N. M. Atkinson, J. S. Kauppila, **T. D. Loveless**, S. E. Armstrong, W. T. Holman, L. W. Massengill, "Single-Event-Hardened CMOS Operational Amplifier Design," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 4, pp. 803-810, Aug. 2012.
- (J27) S. Jagannathan, **T. D. Loveless**, B. L. Bhuvu, S.-J. Wen, R. Wong, M. Sachdev, D. Rennie, and L. W. Massengill, "Single-Event Tolerant Flip-Flop Design in 40-nm Bulk CMOS Technology," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp. 3033-3037, Dec. 2011.
- (J28) J. S. Kauppila, T. D. Haeffner, D. R. Ball, A. V. Kauppila, **T. D. Loveless**, S. Jagannathan, A. L. Sternberg, B. L. Bhuvu, and L. W. Massengill, "Circuit-Level Layout-Aware Single-Event Sensitive-Area Analysis of 40-nm Bulk CMOS Flip-Flops Using Compact Modeling," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp. 2680-2686, Dec. 2011.

- (J29) N. J. Gaspard, A. F. Witulski, N. M. Atkinson, J. R. Ahlbin, W. T. Holman, B. L. Bhuva, **T. D. Loveless**, and L. W. Massengill, "Impact of Well Structure on Single-Event Well Potential Modulation in Bulk CMOS," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp.2614-2620, Dec. 2011.
- (J30) N. N. Mahatme, S. Jagannathan, **T. D. Loveless**, L. W. Massengill, B. L. Bhuva, S.-J. Wen, and R. Wong, "Comparison of Combinational Logic and Sequential Error Rates for a Deep Submicron Process," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp.2719-2725, Dec. 2011.
- (J31) J. R. Ahlbin, N. M. Atkinson, M. J. Gadlage, N. J. Gaspard, B. L. Bhuva, **T. D. Loveless**, E. X. Zhang, L. Chen, and L.W. Massengill, "Influence of N-Well Contact Area on the Pulse Width of Single-Event Transients," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp.2585-2590, Dec. 2011.
- (J32) **T. Daniel Loveless**, S. Jagannathan, T. Reece, J. Chetia, B. L. Bhuva, L. W. Massengill, S-J. Wen, R. Wong, and D. Rennie, "Neutron- and Proton-Induced Single Event Upsets for D- and DICE-Flip/Flop Designs at a 40 nm Technology Node," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 3, pp.1008-1014, June 2011.
- (J33) Sarah Armstrong, **Daniel Loveless**, Jonathan Hicks, Dale McMorrow, and Lloyd W. Massengill, "Phase-Dependent Single-Event Sensitivity Analysis of High-Speed A/MS Circuits Extracted from Asynchronous Measurements," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 3, pp. 1066-1071, June 2011.
- (J34) **T. D. Loveless**, M. L. Alles, D. R. Ball, K. M. Warren, and L. W. Massengill, "Parametric Variability Affecting 45 nm SOI SRAM Single Event Upset Cross-Sections," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3228-3233, Dec. 2010.
- (J35) Pierre Maillard, W. Timothy Holman, **T. Daniel Loveless**, Bharat L. Bhuva, and Lloyd W. Massengill, "An RHBD Technique to Mitigate Missing Pulses in Delay Locked Loops," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3634-3639, Dec. 2010.
- (J36) **T. Daniel Loveless**, Lloyd W. Massengill, W. Timothy Holman, Bharat L. Bhuva, Dale McMorrow, and J. Warner, "A Generalized Linear Model for Single Event Transient Propagation in Phase-Locked Loops," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 5, pp. 2933-2947, Oct. 2010.
- (J37) **T. D. Loveless**, B. D. Olson, B. L. Bhuva, W. T. Holman, C. C. Hafer, and L. W. Massengill, "Analysis of Single-Event Transients in Integer-N Frequency Dividers and Harness Assurance Implications for Phase-Locked Loops," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3489-3498, Dec. 2009.
- (J38) S. E. Armstrong, B. D. Olson, J. Popp, J. Braatz, **T. D. Loveless**, W. T. Holman, D. McMorrow, and L. W. Massengill, "Single Event Transient Error Characterization of a Radiation-Hardened by Design 90 nm SerDes Transmitter Driver," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3463-3468, Dec. 2009.
- (J39) **T. D. Loveless**, L. W. Massengill, B. L. Bhuva, W. T. Holman, M. C. Casey, R. A. Reed, S. A. Nation, D. McMorrow, and J. S. Melinger, "A Probabilistic Analysis Technique Applied to a Radiation-Hardened-by-Design Voltage-Controlled-Oscillator for Mixed-Signal Phase-Locked Loops," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3447-3455, Dec. 2008.

- (J40) O. A. Amusan, P. R. Fleming, B. L. Bhuvu, L. W. Massengill, A. F. Witulski, A. Balasubramanian, M. C. Casey, D. Mcmorrow, S. Nation, F. Barsun, J. S. Melinger, M. Gadlage, and **T. D. Loveless**, “Laser Verification of On-Chip Charge Collection Measurement Circuit,” *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3309-3313, Dec. 2008.
- (J41) A. Balasubramanian, B. L. Bhuvu, L. W. Massengill, B. Narasimham, R. L. Shuler, **T. D. Loveless**, and W. Timothy Holman, “A Built-In Self-Test (BIST) Technique for Hardness Assurance against SETs in Digital Circuits,” *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3130-3135, Dec. 2008.
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- (J46) **T. D. Loveless**, L. W. Massengill, B. L. Bhuvu, W. T. Holman, A. F. Witulski and Y. Boulghassoul, “A Hardened-by-Design Technique for RF Digital Phase-Locked Loops,” *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3432-3438, Dec. 2006.

Conference Proceedings (34, 22 Refereed)

- (C1) (**Refereed**) S. Jagannathan, N. Mahatme, **T. D. Loveless**, B. L. Bhuvu, and L. W. Massengill, “Hardware Based Empirical Model for Predicting Logic Soft Error Cross-Section,” proceedings of the 2016 IEEE International Reliability Physics Symposium (IRPS), Pasadena, CA, pp. 3B.3.1-3B.3.5, Apr. 2016.
- (C2) J. S. Kauppila, **T. D. Loveless**, T. Haeffner, A. L. Sternberg, D. R. Ball, J. Rowe, T. Assis, H. Jiang, H. Zhang, B. L. Bhuvu, M. L. Alles, and L. W. Massengill, “14/16nm FinFET Radiation Response Characterization,” proceedings of the Government Microcircuits Applications and Critical Technology Conference (GOMACTech), Orlando, FL, March, 2016.
- (C3) (**Refereed**) J. A. Maharrey, J. S. Kauppila, R. C. Quinn, **T. D. Loveless**, E. X. Zhang, W. T. Holman, B. L. Bhuvu, and L. W. Massengill, “Heavy-Ion Induced SETs in 32nm SOI Inverter Chains,” 2015 Nuclear Space and Radiation Effects Conference (NSREC) Data Workshop, Boston, MA, July 2015.
- (C4) (**Refereed**) R. C. Quinn, J. S. Kauppila, **T. D. Loveless**, J. A. Maharrey, J. D. Rowe, M. L. Alles, B. L. Bhuvu, R. A. Reed, W. T. Holman, M. Bounasser, K. Lilja, and L. W. Massengill, “Heavy-Ion SEU Test Data for 32 nm SOI Flip-Flops,” 2015 Nuclear Space and Radiation Effects Conference (NSREC) Data Workshop, Boston, MA, July 2015.

- (C5) **(Refereed)** D. McPherson, A. Ofoli, and **T. D. Loveless**, “BasketBallBot: Developing an Intelligent Controls Teaching Platform using LabView, MATLAB, and Arduino,” proceedings of the 2015 IEEE SoutheastCon, Ft. Lauderdale, FL, Apr. 2015.
- (C6) J. Kauppila, J. Maharrey, R. Quinn, **D. Loveless**, T. Haeffner, J. Rowe, D. Ball, M. Alles, and L. Massengill, “Single-Event Measurements and Modeling in 32 nm SOI CMOS,” presented at the Government Microcircuits Applications and Critical Technology Conference (GOMACTech), St. Louis, MO, March, 2015.
- (C7) **(Refereed)** N. N. Mahatme, N. J. Gaspard, T. Assis, **T. D. Loveless**, B. L. Bhuvu, L. W. Massengill, S.-J. Wen, R. Wong, “Impact of Technology Scaling on Combinational Logic Soft Errors,” proceedings of the 2014 IEEE International Reliability Physics Symposium (IRPS), Waikoloa, HI, pp. 5F. 2.1-5F. 2.6, June 2014.
- (C8) **(Refereed)** N. J. Gaspard, S. Jagannathan, Z. Diggins, **T. D. Loveless**, B. L. Bhuvu, L. W. Massengill, W. T. Holman, J. S. Kauppila, S.-J. Wen, R. Wong, “Soft error rate comparison of various hardened and non-hardened flip-flops at 28-nm node,” proceedings of the 2014 IEEE International Reliability Physics Symposium (IRPS), Waikoloa, HI, pp. SE. 5.1-SE. 5.5, June 2014.
- (C9) **(Refereed)** J. S. Kauppila, **T. D. Loveless**, R. C. Quinn, J. A. Maharrey, M. L. Alles, M. McCurdy, R. A. Reed, B. L. Bhuvu, L. W. Massengill, K. Lilja, “Utilizing Device Stacking for Are Efficient Hardened SOI Flip-Flop Designs,” proceedings of the 2014 IEEE International Reliability Physics Symposium (IRPS), Waikoloa, HI, pp. SE. 4.1-SE. 4.7, June 2014.
- (C10) R. C. Quinn, **T. D. Loveless**, J. S. Kauppila, J. A. Maharrey, S. Jagannathan, E. X. Zhang, M. L. Alles, M. W. McCurdy, R. A. Reed, L. W. Massengill, “Use of Alpha Particle and Ion Accelerators for Characterization of Soft-Error Reliability in Advanced ICs,” by, proceedings of the 23rd International Conference on the Application of Accelerators in Research and Industry (CAARI), San Antonio, TX, May 2014.
- (C11) **(Refereed)** N. Gaspard, S. Jagannathan, Z. Diggins, T. Reece, S.-J. Wen, R. Wong, K. Lilja, M. Bounasser, **T. D. Loveless**, W. T. Holman, B. L. Bhuvu, and L. W. Massengill, “Angled flip-flop single-event cross sections for submicron bulk CMOS technologies,” proceedings of the 2013 14th European Conference on Radiation and Its Effects on Components and Systems (RADECS), Oxford, UK, pp. C5.1-C5.4, Sept. 2013.
- (C12) **(Refereed)** N. Gaspard, S. Jagannathan, Z. Diggins, A. V. Kauppila, **T. D. Loveless**, J. S. Kauppila, B. L. Bhuvu, L. W. Massengill, W. T. Holman, A. S. Oates, Y. Fang, S.-J. Wen, and R. Wong, “Effect of Threshold Voltage Implants on Single-Event Error Rates of D-Flip Flops in 28 nm Bulk CMOS,” proceedings of the 2013 IEEE International Reliability Physics Symposium (IRPS), Anaheim, CA, pp. SE.7.1-SE.7.3, April 2013.
- (C13) **(Refereed)** N. Gaspard, S. Jagannathan, Z. Diggins, M. McCurdy, **T. D. Loveless**, B. L. Bhuvu, L. W. Massengill, W. T. Holman, T. S. Oates, Y. Fang, S.-J. Wen, R. Wong, K. Lilja, and M. Bounasser, “Estimation of Hardened Flip-Flops Neutron Soft Error Rates Using SRAM Multiple-Cell Upset Data in Bulk CMOS,” proceedings of the 2013 IEEE International Reliability Physics Symposium (IRPS), Anaheim, CA, pp. SE.6.1-SE.6.5, April 2013.
- (C14) **(Refereed)** N. Mahatme, N. J. Gaspard, S. Jagannathan, T. D. Loveless, H. Abdel-Aziz, B. L. Bhuvu, L. W. Massengill, S. Wen, and R. Wong, “Estimating the Frequency Threshold for Logic Soft Errors,” proceedings of the 2013 IEEE International Reliability Physics Symposium (IRPS), Anaheim, CA, pp. 3D.3.1-3D.3.6, April 2013.

- (C15) W. T. Holman, J. S. Kauppila, **T. D. Loveless**, L. W. Massengill, B. L. Bhuva, and A. F. Witulski, "Low Penalty Radiation-Hardened-by-Design Concepts for High-Performance Analog, Mixed-Signal, and RF Circuits," presented at the Government Microcircuits Applications and Critical Technology Conference (GOMACTech), Las Vegas, NV, March, 2013.
- (C16) (**Refereed**) N. Rezzak, E. X. Zhang, D. R. Ball, M. L. Alles, **T. D. Loveless**, R. D. Schrimpf, and K. P. Rodbell, "Total-ionizing-dose radiation response of 32 nm partially and 45 nm fully-depleted SOI devices," proceedings of the 2012 IEEE International SOI Conference, Oct. 2012
- (C17) (**Refereed**) L. W. Massengill, B. L. Bhuva, W. T. Holman, M. L. Alles, and **T. D. Loveless**, "Technology Scaling and Soft Error Reliability," proceedings of the 2012 IEEE International Reliability Physics Symposium (IRPS), pp. 3C.1.1-3C.1.7, April 2012.
- (C18) (**Refereed**) S. Jagannathan, Z. Diggins, N. Mahatme, **T. D. Loveless**, B. L. Bhuva, S-J. Wen, R. Wong, and L. W. Massengill, "Temperature dependence of soft error rate in flip-flop designs," proceedings of the 2012 IEEE International Reliability Physics Symposium (IRPS), pp. SE.2.1-SE.2.6, April 2012.
- (C19) (**Refereed**) I. Chatterjee, S. Jagannathan, **D. Loveless**, B. L. Bhuva, S. Wen, R. Wong, M. Sachdev, "Impact of well contacts on the single event response of radiation-hardened 40-nm flip-flops," proceedings of the 2012 IEEE International Reliability Physics Symposium (IRPS), pp. SE.4.1-SE.4.6, April 2012.
- (C20) **D. Loveless**, J. Kauppila, T. Haeffner, T. Holman, M. Alles, B. Bhuva, L. Massengill, S. Jagannathan, N. Gaspard, N. Atkinson, R. Blaine, J. Ahlbin, "Analysis of Single-Event Transients in a 45-nm SOI Technology for Rad-Hard Applications," proceedings of the Government Microcircuits Applications and Critical Technology Conference (GOMACTech), Las Vegas, NV, March, 2012.
- (C21) P. Maillard, **T. D. Loveless**, W. T. Holman, L. W. Massengill, "Design Choices for High-Speed RHBD Delay-Locked Loops," proceedings of the Government Microcircuits Application Conference, Las Vegas, NV, March, 2012.
- (C22) R. W. Blaine, N. M. Atkinson, J. S. Kauppila, S. E. Armstrong, **T. D. Loveless**, W. T. Holman, L. W. Massengill, "Single-Event Hardening Techniques for CMOS Operational Amplifier Design," proceedings of the Government Microcircuits Application Conference, Las Vegas, NV, March, 2012.
- (C23) (**Refereed**) M. L. Alles, R. D. Schrimpf, R. A. Reed, L. W. Massengill, R. A. Weller, M. H. Mendenhall, D. R. Ball, K. M. Warren, **T. D. Loveless**, J. S. Kauppila, and B. D. Sierawski, "Radiation Hardness of FDSOI and FinFET technologies," proceedings of the 2011 IEEE International SOI Conference, Oct. 2011.
- (C24) (**Refereed**) P. Maillard, **T. D. Loveless**, W. T. Holman, and L. W. Massengill, "A Radiation-Hardened Delay-Locked Loop Design (DLL) Utilizing Differential Delay Lines Topology," proceedings of the 12th European Conference on Radiation Effects on Components and Systems (RADECS), Sept. 2011.
- (C25) (**Refereed**) J. R. Ahlbin, **T. D. Loveless**, D. R. Ball, B. L. Bhuva, A. F. Witulski, L. W. Massengill, M. J. Gadlage, "Double-pulse-single-event transients in combinational logic," proceedings of 2011 IEEE International Reliability Physics Symposium (IRPS), pp. 3C.5.1-3C.5.6, April 2011.

- (C26) **(Refereed)** S. Jagannathan, **T. D. Loveless**, T. Reece, B. L. Bhuva, , S-J. Wen, R. Wong, L. W. Massengill, “Neutron and Alpha Particles Induced Soft-Error Rates for Flip Flops at a 40 nm Technology Node,” proceedings of the 2011 IEEE International Reliability Physics Symposium (IRPS), pp. SE.5.1-SE.5.5, April 2011.
- (C27) **T. Daniel Loveless**, W. Timothy Holman, Bharat L. Bhuva, Lloyd W. Massengill, Jonathan R. Ahlbin, Nick M. Atkinson, En Xia Zhang, Nelson Gaspard, Pierre Maillard, Matthew J. Gadlage, Oluwole A. Amusan, and Megan C. Casey, “Single-Event Effects Characterization of Analog, Digital, and Low-Power Electronics Designed in a Multiple-Tiered SOI Process,” proceedings of the Government Microcircuits Applications and Critical Technology Conference (GOMACTech), Mar. 2011.
- (C28) Jeffrey S. Kauppila, Andrew L. Sternberg, Michael L. Alles, **T. Daniel Loveless**, Bharat L. Bhuva, W. Timothy Holman, and Lloyd W. Massengill, “Radiation-Enabled Compact Models for Advanced Technology Integrated Circuit Design,” proceedings of the Government Microcircuits Applications and Critical Technology Conference (GOMACTech), Mar. 2011.
- (C29) **(Refereed)** B. L. Bhuva, K. Lilja, J. Holts, S. J. Wen, R. Wong, S. Jagannathan, **T. D. Loveless**, M. McCurdy, and Z. J. Diggins, “Comparative Analysis of Flip-Flop Designs for Soft Errors at Advanced Technology Nodes,” proceedings of the 2011 IEEE International Conference on IC Design & Technology (ICICDT), May 2011.
- (C30) J. S. Kauppila, A. L. Sternberg, M. L. Alles, **T. D. Loveless**, B. L. Bhuva, W. T. Holman, and L. W. Massengill, “Radiation-Enabled Compact Modes for Advanced Technology Integrated Circuit Design,” proceedings of the Government Microcircuits Applications and Critical Technology Conference (GOMACTech), Orlando, FL, March, 2011.
- (C31) **T. Daniel Loveless**, Lloyd W. Massengill, W. Timothy Holman, and Bharat L. Bhuva, “Single-Event Hardening of High-Speed Mixed-Signal Circuits,” proceedings of the Government Microcircuits Applications and Critical Technology Conference (GOMACTech), Reno, NV, March, 2010.
- (C32) W. T. Holman, L. W. Massengill, B. L. Bhuva, A. W. Witulski, and **T. D. Loveless**, “Recent Advances in Radiation-Hardened-by-Design Analog and Mixed-Signal Circuits,” proceedings of the Government Microcircuits Applications and Critical Technology Conference (GOMACTech), Reno, NV, March, 2010.
- (C33) **(Refereed)** A. V. Kauppila, **T. D. Loveless**, G. L. Vaughn, B. L. Bhuva, L. W. Massengill, and W. T. Holman, “Analysis of the Single-Event Effects of a 90nm CMOS Phase-Locked Loop,” proceedings of the 10th European Conference on Radiation Effects on Components and Systems (RADECS), pp. 201-206, September 2009.
- (C34) **(Refereed)** Megan C. Casey, Bharat L. Bhuva, Sarah A. Nation, Oluwole A. Amusan, **T. Daniel Loveless**, Lloyd W. Massengill, Dale McMorrow and Joseph S. Melinger, “Single-Event Effects on Ultra-Low Power CMOS Circuits,” proceedings of the 2009 IEEE International Reliability Physics Symposium (IRPS), pp. 194-198, April 2009.

Thesis and Dissertation

T. D. Loveless, “A Generalized Single-Event Analysis and Hardening Options for Mixed-Signal Phase-Locked Loop Circuits,” *Ph.D. Dissertation*, Vanderbilt University, Aug. 2009.

T. D. Loveless, “A Radiation-Hardened -by-Design Charge Pump for Phase-Locked-Loop Circuits,” *M.S. Thesis*, Vanderbilt University, Mar. 2007.

Book Chapters (3)

Loveless, T. D. and Holman, W. T. (2015). Single-Event Mitigation Techniques for Analog and Mixed-Signal Circuits. In M. Bagatin & Gerardin (Eds.), *Ionizing Radiation Effects in Electronics: From Memories to Imagers* (Chp. 9).

Loveless, T. D. (2012). CMOS Phase Locked Loops. In J. D. Cressler, & A. Mantooth (Eds.), *Extreme Environment Electronics* (pp. 601-618).

Loveless, T. D. (2011). Analogue and Mixed-Signal Circuits. In ESA-ESTEC (ESA Requirements and Standard Division), *Space engineering, product assurance: Techniques for Radiation Effects Mitigation in ASICs and FPGAs*, Dec. 2011.

XI. Conference Presentations (without proceeding or associated publication):

Invited Talks/Lectures (13)

- (11) *INVITED* “Hardening-By-Design Techniques for Analog and Mixed-Signal ASICs,” by **T. D. Loveless**, presented at the 12th International School on the Effects of Radiation on Embedded Systems for Space Applications (SERESSA), Munich, Germany, Oct. 2017.
- (12) *INVITED* “Hardening-By-Design Techniques for Analog and Mixed-Signal ASICs,” by **T. D. Loveless**, presented at the 12th International School on the Effects of Radiation on Embedded Systems for Space Applications (SERESSA), Montreal, Quebec, Canada, Nov. 2016.
- (13) *INVITED* “Radiation Effects and Basic Mitigation Techniques for Mixed-Signal Electronics,” by **T. D. Loveless**, presented at the 2016 Hardened Electronics and Radiation Technology (HEART) Conference, Monterey, CA, Apr. 2016.
- (14) *INVITED* “Embedded Systems and Small Satellites for Smart Cities,” by **T. D. Loveless**, presented at the US Ignite Technical Interchange, UTC, Chattanooga, TN, Mar. 2016.
- (15) *INVITED* “Hardening-By-Design Techniques for Analog and Mixed-Signal ASICs,” by **T. D. Loveless**, presented at the 11th International School on the Effects of Radiation on Embedded Systems for Space Applications (SERESSA), Puebla, Mexico, Dec. 2015.
- (16) *INVITED*, “RHBD Body-Driven Circuits for Low-Voltage AMS Systems”, by **T. D. Loveless**, presented at the DTRA Radiation Effects Review, NRO Nanoscale Rad-Hard Review, General RHBD Technical Interchange Meeting Vanderbilt University, Nashville, TN, May 12-13, 2015.
- (17) *INVITED*, “Single-Event Mitigation Techniques for Analog and Mixed-Signal ASICs,” by **Daniel Loveless**, presented at the 7th International School on the Effects of Radiation on Embedded Systems for Space Applications (SERESSA), Toulouse, France, Dec. 2011.
- (18) *INVITED* “Neutron-Induced Soft-Error Rate Measurements in 40 nm Bulk CMOS,” by Daniel Loveless, presented at JEDEC G12 RHA Users Subcommittee Meeting, Tempe, AZ, Feb. 2011.
- (19) *INVITED*, “Single-Event Mitigation Techniques for Analog and Mixed-Signal ASICs,” by **Daniel Loveless**, presented at the 6th International School on the Effects of Radiation on Embedded Systems for Space Applications (SERESSA), São José Dos Campos, Brazil, Dec. 2010.

- (I10) *INVITED*, “Basic Radiation Effects Analysis, Modeling, and Hardening-by-Design,” by **Daniel Loveless**, presented at the 6th International School on the Effects of Radiation on Embedded Systems for Space Applications (SERESSA), São José Dos Campos, Brazil, Dec. 2010.
- (I11) *INVITED* “Mitigation Techniques for Analog and Mixed-Signal ASICs,” by Daniel Loveless, presented at the Workshop on Mitigation Techniques Against Radiation on Integrated Circuits, the Space Research and Technology Centre of the European Space Agency (ESA/ESTEC), Noordwijk, The Netherlands, Sept. 2010.
- (I12) *INVITED* “Basics Part II: An Overview of Radiation Effects Analysis,” by **T. D. Loveless** and S. E. Armstrong, presented at the 5th International School on the Effects of Radiation on Embedded Systems for Space Applications (SERESSA), Takasaki, Japan, Dec. 2009.
- (I13) *INVITED* “Basics Part I: Devices and Circuits for Radiation Environments,” by S. E. Armstrong and **T. D. Loveless**, presented at the 5th International School on the Effects of Radiation on Embedded Systems for Space Applications (SERESSA), Takasaki, Japan, Dec. 2009.

Other (65)

- (P1) “Efficacy of Fuzzy Electronics in Space,” by S. Singh and **T. D. Loveless**, presented at the 52nd Annual Conference of the National Collegiate Honors Council (NCHC), Atlanta, GA, Nov. 2017.
- (P2) “Undergraduate Research Experience in the Space Sciences,” by **T. D. Loveless**, presented at the WCTL Instructional Excellence Conference, Chattanooga, TN, May 2017.
- (P3) “UTChattSat: Space Science and Engineering in the Classroom,” by **T. D. Loveless** and A. M. Patel, presented at the StartupCHA Week/Co.Lab Demo Night, Chattanooga, TN, Oct. 2016.
- (P4) “UTChattSat,” by **T. D. Loveless**, M. B. Joplin, A. M. Patel, and D. Johnson, presented at the GIGTank365 boutique accelerator pitch night, Chattanooga, TN, July 2016.
- (P5) “A Single-Event Transient Measurement Payload for a 1U CubeSat,” by M. B. Joplin, **T. D. Loveless**, J. S. Kauppila, and L. W. Massengill, presented at the 2016 Single-Event Effects Symposium, La Jolla, CA, May 2016.
- (P6) “Radiation and Reliability Resiliency of Advanced and Emerging Integrated Circuit Technologies,” by **T. D. Loveless**, M. B. Joplin, and A. M. Patel, presented at the 2016 University of Tennessee at Chattanooga Research Dialogues, Apr. 2016.
- (P7) “Rocket Scientist, Engineer, and Educator,” by **T. D. Loveless**, presented at the 2016 University of Tennessee at Chattanooga Research Dialogues Faculty Elevator Speech Competition, Apr. 2016.
- (P8) “Frequency Trends Observed in 32 nm SOI Flip-Flops and Combinational Logic,” by R. C. Quinn, J. S. Kauppila, **T. D. Loveless**, J. A. Maharrey, J. D. Rowe, M. W. McCurdy, M. L. Alles, B. L. Bhuva, R. A. Reed, K. Lilja, and L. W. Massengill, presented at the 2015 Nuclear Space and Radiation Effects Conference (NSREC), Boston, MA, July 2015.

- (P9) “Layout based RHBD for Sequential and Combinatorial Logic,” by K. Lilja, M. Bounasser, R.C. Quinn, J. S. Kauppila, **T. D. Loveless**, J.A. Maharrey, J.D. Rowe, M.W. McCurdy, M.L. Alles, B.L. Bhuvu, R.A. Reed, and L. W. Massengill, presented at the 2015 Single-Event Effects Symposium, La Jolla, CA, May 2015.
- (P10) “Power-Aware Mitigation of Combinational Logic Soft Errors,” by N. N. Mahatme, N. J. Gaspard, T. Assis, **T. D. Loveless**, B.L. Bhuvu, W. H. Robinson, L. W. Massengill, S.-J. Wen, R. Wong, presented at the 2014 Nuclear Space and Radiation Effects Conference (NSREC), Paris, FR, July 2014.
- (P11) “Identification of a Pulse-Width Window of Vulnerability for Single-Event-Transient-Induced Harmonic Errors in Ring Oscillators,” by Y. P. Chen, **T. D. Loveless**, P. Maillard, N. J. Gaspard, S. Jagannathan, A. F. Witulski, B. L. Bhuvu, W. T. Holman, L. W. Massengill, presented at the 23rd Annual Single Event Effects (SEE) Symposium, La Jolla, CA, May 2014.
- (P12) “Use of Alpha Particle and Ion Accelerators for Characterization of Soft-Error Reliability in Advanced ICs,” by R. C. Quinn, **T. D. Loveless**, J. S. Kauppila, J. A. Maharrey, S. Jagannathan, E. X. Zhang, M. L. Alles, M. W. McCurdy, R. A. Reed, L. W. Massengill, presented at the 23rd International Conference on the Application of Accelerators in Research and Industry (CAARI), San Antonio, TX, May 2014.
- (P13) “Single-Event Transient (SET) Analysis of 40 nm Digital-Controlled Oscillator (DCO) Topologies,” by Y. Chen, **T. D. Loveless**, P. Maillard, S. Jagannathan, N. Gaspard, N. M. Atkinson, and L. W. Massengill, presented at the 22nd Annual Single Event Effects (SEE) Symposium, La Jolla, CA, April 2013.
- (P14) “Single Event Investigations of a 40 nm Low Noise Amplifier,” by K. Freeman, S. Jagannathan, **T. D. Loveless**, N. J. Gaspard, N. M. Atkinson, P. Maillard, J. S. Kauppila, and L. W. Massengill, presented at the 22nd Annual Single Event Effects (SEE) Symposium, La Jolla, CA, April 2013.
- (P15) “A New Error Correction Circuit for Delay Locked Loops,” by P. Maillard, W. T. Holman, **T. D. Loveless**, and L. W. Massengill, presented at the 22nd Annual Single Event Effects (SEE) Symposium, La Jolla, CA, April 2013.
- (P16) “SET Pulse Width Trends in Highly Scaled SOI,” by R. C. Quinn, J. A. Maharrey, **T. D. Loveless**, J. S. Kauppila, S. Jagannathan, N. M. Atkinson, N. J. Gaspard, E. Zhang, W. T. Holman, B. L. Bhuvu, and L. W. Massengill, presented at the 22nd Annual Single Event Effects (SEE) Symposium, La Jolla, CA, April 2013.
- (P17) “Effect of Negative Bias Temperature Instability on the Single Event Upset Response of 40 nm Flip-Flops,” by A. V. Kauppila, B. L. Bhuvu, **T. D. Loveless**, S. Jagannathan, N. J. Gaspard, J. S. Kauppila, L. W. Massengill, S.-J. Wen, R. Wong, G. L. Vaughn, and W. T. Holman, presented at the 2012 Nuclear and Space Radiation Effects Conference (NSREC), Miami, FL, July 2012.
- (P18) “On-Chip Measurement of Single-Event Transients in a 45 nm Silicon-on-Insulator Technology,” by **T. D. Loveless**, J. S. Kauppila, S. Jagannathan, D. R. Ball, J. D. Rowe, N. J. Gaspard, N. M. Atkinson, R. W. Blaine, T. R. Reece, J. R. Ahlbin, T. D. Haeffner, M. L. Alles, W. T. Holman, B. L. Bhuvu, L. W. Massengill, presented at the 2012 Nuclear and Space Radiation Effects Conference (NSREC), Miami, FL, July 2012.

- (P19) “Frequency Dependence of Alpha-Particle Induced Soft Error Rates of Flip-Flops in 40-nm CMOS Technology,” by S. Jagannathan, **T. D. Loveless**, B. L. Bhuvan, N. J. Gaspard, N. Mahatme, T. Assis, S-J. Wen, R. Wong, and L. W. Massengill, presented at the 2012 Nuclear and Space Radiation Effects Conference (NSREC), Miami, FL, July 2012.
- (P20) “Differential Charge Cancellation (DCC) Layout as an RHBD Technique for Bulk CMOS Differential Circuit Design,” by R. W. Blaine, N. M. Atkinson, J. S. Kauppila, S. E. Armstrong, N. C. Hooten, **T. D. Loveless**, J. H. Warner, W. T. Holman, L. W. Massengill, presented at the 2012 Nuclear and Space Radiation Effects Conference (NSREC), Miami, FL, July 2012.
- (P21) “Evaluation of Built-In-Self-Test Circuitry for Single-Event Transient Measurements in 45 nm SOI,” by **T. D. Loveless**, J. S. Kauppila, D. R. Ball, S. Jagannathan, T. D. Haeffner, N. J. Gaspard, N. M. Atkinson, R. W. Blaine, T. R. Reece, M. L. Alles, W. T. Holman, B. L. Bhuvan, and L. W. Massengill, presented at the 21st Annual Single Event Effects (SEE) Symposium, La Jolla, CA, April 2012.
- (P22) “The Quad-Path Hardening Technique for Switched-Capacitor Circuits,” by N. M. Atkinson, W. T. Holman, J. S. Kauppila, R. W. Blaine, **T. D. Loveless**, and L. W. Massengill, presented at the 21st Annual Single Event Effects (SEE) Symposium, La Jolla, CA, April 2012.
- (P23) “RHBD Techniques for CMOS Operational Amplifier Design,” by R. W. Blaine, N. M. Atkinson, J. S. Kauppila, **T. D. Loveless**, S. E. Armstrong, W. T. Holman, and L. W. Massengill, presented at the 21st Annual Single Event Effects (SEE) Symposium, La Jolla, CA, April 2012.
- (P24) “Frequency Dependence of Alpha-Particle Induced Soft Error Rates of Flip-Flops in 40 nm CMOS Technology,” by S. Jagannathan, **T. D. Loveless**, N. J. Gaspard, B. L. Bhuvan, T. Assis, Z. J. Diggins, S-J. Wen, R. Wong, and L. W. Massengill, presented at the 21st Annual Single Event Effects (SEE) Symposium, La Jolla, CA, April 2012.
- (P25) “SET Characterization of Two 90 nm Voltage Controlled Delay Line (VCDL) Topologies,” by P. Maillard, L. W. Massengill, W. T. Holman, **T. D. Loveless**, Y. Chen, N. Roche, J. Warner, S. Buchner, and D. McMorro, presented at the 21st Annual Single Event Effects (SEE) Symposium, La Jolla, CA, April 2012.
- (P26) “Analysis of Single-Event Transients in a 45 nm SOI Technology for Rad-Hard Applications,” by **D. Loveless**, J. Kauppila, T. Haeffner, T. Holman, M. Alles, B. Bhuvan, L. Massengill, S. Jagannathan, N. Gaspard, N. Atkinson, R. Blaine, J. Ahlbin, presented at the 37th Annual Government Microcircuit Applications & Critical Technology Conference (GOMACTech), Las Vegas, NV, March 2012.
- (P27) “Design Choices for High Speed Radiation-Hardened Delay-Locked Loops,” by Pierre Maillard, **T. Daniel Loveless**, W. Timothy Holman, and Lloyd W. Massengill, presented at the 37th Annual Government Microcircuit Applications & Critical Technology Conference (GOMACTech), Las Vegas, NV, March 2012.
- (P28) “Single-Event Hardening Techniques for CMOS Operational Amplifier Design,” by R. W. Blaine, N. M. Atkinson, J. S. Kauppila, S. E. Armstrong, **T. Daniel Loveless**, W. Timothy Holman, and Lloyd W. Massengill, presented at the 37th Annual Government Microcircuit Applications & Critical Technology Conference (GOMACTech), Las Vegas, NV, March 2012.

- (P29) “Single-Event-Hardened CMOS Operational Amplifier Design,” by R. W. Blaine, S. E. Armstrong, N. M. Atkinson, J. S. Kauppila, **T. D. Loveless**, W. T. Holman, and L. W. Massengill, presented at the 12th European Conference on Radiation Effects on Components and Systems (RADECS), Seville, Spain, Sept. 2011.
- (P30) “Single-Event Tolerant Flip-Flop Design in 40 nm CMOS Technology,” by S. Jagannathan, **T. D. Loveless**, J. R. Ahlbin, B. L. Bhuvu, S-J. Wen, R. Wong, M. Sachdev, D. Rennie, and L. W. Massengill, presented at the 2011 Nuclear and Space Radiation Effects Conference (NSREC), Las Vegas, NV, July 2011.
- (P31) “Influence of N-Well Contact Area on the Pulse Width of Single-Event Transients,” by J. R. Ahlbin, N. M. Atkinson, M. J. Gadlage, N. J. Gaspard, B. L. Bhuvu, **T. D. Loveless**, E. X. Zhang, L. Chen, and L.W. Massengill, presented at the 2011 Nuclear and Space Radiation Effects Conference (NSREC), Las Vegas, NV, July 2011.
- (P32) “Circuit-Level Layout-Aware Single-Event Sensitive-Area Analysis of 40 nm Bul CMOS Flip-Flops Using Compact Modeling,” by J. S. Kauppila, T. D. Haeffner, D. R. Ball, A. V. Kauppila, **T. D. Loveless**, S. Jagannathan, A. L. Sternberg, B. L. Bhuvu, and L. W. Massengill, presented at the 2011 Nuclear and Space Radiation Effects Conference (NSREC), Las Vegas, NV, July 2011.
- (P33) “Comparison of Combinational and Sequential Error Rates for a Deep Submicron Process,” by N. N. Mahatme, S. Jagannathan, **T. D. Loveless**, L. W. Massengill, B. L. Bhuvu, S.-J. Wen, R. Wong, presented at the 2011 Nuclear and Space Radiation Effects Conference (NSREC), Las Vegas, NV, July 2011.
- (P34) “Impact of Well Structure on Single-Event Well Potential Modulation in Bulk CMOS,” by N. J. Gaspard, A. F. Witulski, N. M. Atkinson, J. R. Ahlbin, W. T. Holman, B. L. Bhuvu, **T. D. Loveless**, and L. W. Massengill, presented at the 2011 Nuclear and Space Radiation Effects Conference (NSREC), Las Vegas, NV, July 2011.
- (P35) “Single-Event Vulnerability of Mixed-Signal Circuit Interfaces in Communication Devices,” by S. E. Armstrong, **T. D. Loveless**, R. W. Blaine, N. M. Atkinson, W. T. Holman, and L. W. Massengill, presented at the 20th Annual Single Event Effects (SEE) Symposium, La Jolla, CA, April 2011.
- (P36) “A Radiation-Hardened Delay-Locked Loop Design Utilizing Differential Delay Line Topology,” by P. Maillard, **T. D. Loveless**, W. T. Holman, and L. W. Massengill, presented at the 20th Annual Single Event Effects (SEE) Symposium, La Jolla, CA, April 2011.
- (P37) “Effect of Latchup Mitigation Techniques on Well Potential Modulation and Single-Event-Transient Pulse Widths,” by N. J. Gaspard, A. F. Witulski, N. M. Atkinson, J. R. Ahlbin, W. T. Holman, **T. D. Loveless**, B. L. Bhuvu, and L. W. Massengill, presented at the 20th Annual Single Event Effects (SEE) Symposium, La Jolla, CA, April 2011.
- (P38) “Neutron- and Proton-Induced SEU Error Rates for D- and DICE-Flip/Flop designs at a 40 nm Technology Node,” by **T. Daniel Loveless**, S. Jagannathan, T. Reece, J. Chetia, B. L. Bhuvu, L. W. Massengill, S-J. Wen, R. Wong, and D. Rennie, presented at the 11th European Conference on Radiation Effects on Components and Systems (RADECS), Sept. 2010.

- (P39) “Phase-Dependent Single-Event Sensitivity Analysis of High-Speed A/MS Circuits Extracted from Asynchronous Measurements,” by Sarah Armstrong, **Daniel Loveless**, Jonathan Hicks, Dale McMorrow, and Lloyd W. Massengill, presented at the 11th European Conference on Radiation Effects on Components and Systems (RADECS), Sept. 2010.
- (P40) “Variables Affecting the Low LET SEU Cross Sections of a 45 nm CMOS SOI SRAM,” by **T. D. Loveless**, M. L. Alles, D. R. Ball, K. M. Warren, and L. W. Massengill, presented at the 2010 Nuclear and Space Radiation Effects Conference (NSREC), Denver, CO, July 2010.
- (P41) “An RHBD Technique to Mitigate Missing Pulses in Delay Locked Loops,” by Pierre Maillard, W. T. Holman, **T. D. Loveless**, B. L. Bhuvu, and L. W. Massengill, presented at the 2010 Nuclear and Space Radiation Effects Conference (NSREC), Denver, CO, July 2010.
- (P42) “A Generalized Model for Single-Event Analysis and Hardening of Mixed-Signal Phase-Locked Loops,” by **T. Daniel Loveless**, Lloyd W. Massengill, W. Timothy Holman, Bharat L. Bhuvu, Dale McMorrow, and Jeff Warner, presented at the 19th Annual Single Event Effects (SEE) Symposium, San Diego, CA, April 2010.
- (P43) “Experimental Extraction of Phase-Dependent Single-Event Sensitivity,” by S. E. Armstrong, **T. D. Loveless**, J. R. Hicks, D. McMorrow, and L. W. Massengill, presented at the 19th Annual Single Event Effects (SEE) Symposium, San Diego, CA, April 2010.
- (P44) “An RHBD Technique to Mitigate Missing Pulses in Delay Locked Loops,” by Pierre Maillard, W. T. Holman, **T. D. Loveless**, B. L. Bhuvu, and L. W. Massengill, presented at the 19th Annual Single Event Effects (SEE) Symposium, San Diego, CA, April 2010.
- (P45) “Single-Event Hardening of High-Speed Mixed-Signal Circuits,” by **T. Daniel Loveless**, Lloyd W. Massengill, W. Timothy Holman, and Bharat L. Bhuvu, presented at the 35th Annual Government Microcircuit Applications & Critical Technology Conference (GOMACTech), Reno, NV, March 2010.
- (P46) “Recent Advances in Radiation-Hardened-by-Design Analog and Mixed-Signal Circuits,” by W. T. Holman, L. W. Massengill, B. L. Bhuvu, A. W. Witulski, and **T. D. Loveless**, presented at the 35th Annual Government Microcircuit Applications & Critical Technology Conference (GOMACTech), Reno, NV, March 2010.
- (P47) “Analysis of Single-Event Transients in Integer-N Frequency Dividers and Impacts on Phase-Locked Loop Performance,” by **T. D. Loveless**, B. L. Bhuvu, W. T. Holman, B. D. Olson, and L. W. Massengill, presented at the 2009 Nuclear and Space Radiation Effects Conference (NSREC), Tucson, AZ, July 2009.
- (P48) “Single-Event-Transient Analysis of Delay-Locked Loops,” by P. Maillard, **T. D. Loveless**, W. T. Holman, B. L. Bhuvu, and L. W. Massengill, presented at the 2008 Nuclear and Space Radiation Effects Conference (NSREC), Tucson, AZ, July 2009.
- (P49) “Analysis and Testing of a Radiation Hardened by Design SerDes Transmitter Driver in 90nm CMOS,” by S. E. Armstrong, B. D. Olson, J. Popp, J. Braatz, **T. D. Loveless**, W. T. Holman, D. McMorrow, and L. W. Massengill, presented at the 2008 Nuclear and Space Radiation Effects Conference (NSREC), Tucson, AZ, July 2009.

- (P50) “Single-Event Effects in Microelectronics Induced by Through-Wafer Sub-Bandgap Two-Photon Absorption,” by Dale McMorrow, William T. Lotshaw, Joseph S. Melinger, Jeffrey Warner, Jonathan Pellish, **T. Daniel Loveless**, Sarah E. Armstrong, Robert Reed, and Lloyd W. Massengill, presented at the 2009 Nonlinear Optics: Materials, Fundamentals and Applications (NLO) Conference, Honolulu, HI, July 2009.
- (P51) “Analysis and Testing of a Radiation Hardened by Design SerDes Transmitter Driver in 90nm CMOS,” by S. Armstrong, J. Popp, J. Braatz, B. D. Olson, **T. D. Loveless**, and L. W. Massengill, presented at the 2009 Single Event Effects (SEE) Symposium, San Diego, La Jolla, CA, April 2009.
- (P52) “Single-Event-Transient Analysis of Delay-Locked Loops,” by P. Maillard, **T. D. Loveless**, W. T. Holman, B. L. Bhuvu, and L. W. Massengill, presented at the 2009 Single Event Effects (SEE) Symposium, San Diego, La Jolla, CA, April 2009.
- (P53) “A Radiation-Hardened-by-Design Voltage-Controlled-Oscillator for Mixed-Signal Phase-Locked Loops” by **T. D. Loveless**, L.W. Massengill, B.L. Bhuvu, and W.T. Holman, presented at the 2008 Nuclear and Space Radiation Effects Conference (NSREC), Tucson, AZ, July 2008.
- (P54) “Laser Verification of On-Chip Charge Collection Measurement Circuit” by O. A. Amusan, P. R. Fleming, B. L. Bhuvu, L.W. Massengill, A. F. Witulski, A. Balasubramanian, M. C. Casey, D. McMorrow, S. Nation, F. Barsun, J. S. Melinger, M. Gadlage, and **T. D. Loveless**, presented at the 2008 Nuclear and Space Radiation Effects Conference (NSREC), Tucson, AZ, July 2008.
- (P55) “A Built-In Self-Test (BIST) Technique for Hardness Assurance against SETs in Digital Circuits” by A. Balasubramanian, B. L. Bhuvu, L. W. Massengill, B. Narasimham, R. L. Shuler, **T. D. Loveless**, and W. Timothy Holman, presented at the 2008 Nuclear and Space Radiation Effects Conference (NSREC), Tucson, AZ, July 2008.
- (P56) “Single-Event Effects on Combinational Logic Circuits Operating at Ultra-Low Power” by M. C. Casey, O. A. Amusan, S. A. Nation, **T. D. Loveless**, A. Balasubramanian, B. L. Bhuvu, R. A. Reed, D. McMorrow, R. A. Weller, M. L. Alles, L. W. Massengill, J. S. Melinger, and B. Narasimham, presented at the 2008 Nuclear and Space Radiation Effects Conference (NSREC), Tucson, AZ, July 2008.
- (P57) “Pulsed Laser Single-Event Effects in Highly Scaled CMOS Technologies in the Presence of Dense Metal Coverage” by A. Balasubramanian, D. McMorrow, S. A. Nation, B. L. Bhuvu, R. A. Reed, L. W. Massengill, **T. D. Loveless**, O. A. Amusan, J. D. Black, J. S. Melinger, M. P. Baze, V. Ferlet-Cavrois, M. Gaillardin, and J. R. Schwank, presented at the 2008 Nuclear and Space Radiation Effects Conference (NSREC), Tucson, AZ, July 2008.
- (P58) “A Radiation-Hardened-by-Design Voltage-Controlled-Oscillator for Mixed-Signal Phase-Locked Loops” by **T. D. Loveless**, L.W. Massengill, B.L. Bhuvu, and W.T. Holman, presented at the 2008 Single Event Effects (SEE) Symposium, Long Beach, CA, April 2008.
- (P59) “Single-Event Effects Induced by Through-Wafer Sub-Bandgap Two-Photon Absorption,” by D. McMorrow, W. T. Lotshaw, J. S. Melinger, P. Jenkins, P. Eaton, J. Benedetto, M. Gadlage, J. D. Davis, R. K. Lawrence, **D. Loveless**, and L. Massengill, presented at the 2007 Nonlinear Optics: Materials, Fundamentals and Applications (NLO) Conference, Kona, Hawaii, July 2007.

- (P60) “Mitigation and Modeling of Single-Event Transients in Voltage-Controlled Oscillators,” by **T. D. Loveless**, L. W. Massengill, W. T. Holman, and B. L. Bhuvan, presented at the 2007 Nuclear and Space Radiation Effects Conference (NSREC), Honolulu, HI, July 2007.
- (P61) “A Single-Event-Hardened Phase-Locked Loop Fabricated in 130nm CMOS,” by **T. D. Loveless**, L. W. Massengill, B. L. Bhuvan, W. T. Holman, R. A. Reed, D. McMorrow, and J. S. Melinger, presented at the 2007 Nuclear and Space Radiation Effects Conference (NSREC), Honolulu, HI, July 2007.
- (P62) “Effects of Technology Scaling on the Single-Event-Transient Response of Phase-Locked Loop Circuits,” by **T. D. Loveless**, B. L. Bhuvan, L. W. Massengill, and W. T. Holman, presented at the 2007 Single Event Effects (SEE) Symposium, Long Beach, CA, April 2007.
- (P63) “A Hardened-by-Design Technique for RF Digital Phase-Locked Loops,” by **T. D. Loveless**, L. W. Massengill, B. L. Bhuvan, W. T. Holman, A. F. Witulski and Y. Boulghassoul, presented at the 2006 Nuclear and Space Radiation Effects Conference (NSREC), Ponte Vedra, FL, July 2006.
- (P64) “Hardening Options for a RF Digital PLL,” by **T. D. Loveless**, L. W. Massengill, B. L. Bhuvan, W. T. Holman, A. F. Witulski, and Y. Boulghassoul, presented at the 2006 Single Event Effects (SEE) Symposium, Long Beach, CA, April 2006.
- (P65) “The Effect of Random Dopant Fluctuations (RDF) on the Radiation Hardness of CMOS Memory Cells,” by A. Balasubramanian, A.L. Sternberg, P.R. Fleming, B.L. Bhuvan, S. Kalemeris, and L.W. Massengill, presented by **T. D. Loveless** at the 2006 Single Event Effects (SEE) Symposium, Long Beach, CA, April 2006.